input data left three pieces) is output.

Next, the data path configuration of the threshold data selection control circuit 14 for generating a barrel shifter control signal SFT and an output selection signal RL will be discussed with reference to FIG. 31. In the figure, the threshold data selection control circuit 14 comprises a register 45 for storing the value of ts, a divider 46 for performing operation of cx0modts, a register 48 for storing the value of ts/2 (when ts is even) or the value of (ts-1)/2 (when ts is odd), a comparator 49 for comparing the remainder output from the divider 46 with the value stored in the register 48 with respect to the greater-than or less-than relationship therebetween, a subtracter 50 for subtracting the remainder output from the divider 46 from the value stored in the register 48, and a selector 51 for selectively outputting the remainder output from the divider 46 or the subtraction result of the subtracter 50 in response to the output of the compactor 49. The significant bit width ss of the remainder or the subtraction result output from the selector 51 is ss≤8 in FIG. 31. In the configuration, the output result of the comparator 49 is output as the output selection signal RL and the remainder or the complement of the remainder output from the selector 51 is output as the barrel shifter control signal SFT.

The hardware configuration of the embodiment has been described. According to the configuration of the embodiment, the

DFF180q. 180-bit binary matrix data SDo is retained in those flip-flop circuits and then is output to a barrel shifter 32q to be described later. (The 180-bit binary matrix data SDo is read out of the binary matrix data storage memory 10q when the fetch timing signal DFT is applied as a clock signal to the flip-flop circuits DFF1 to DFF180q.)

<Selecting and Outputting of Binary Matrix Data>

The binary matrix data selection means 30q (Fig. 38) includes a binary-matrix-data select control circuit 31q, the barrel shifter 32q and a binary matrix data register 33q. To correct a shift of a pixel position of the painting object in the main scanning direction relative to a pixel position of the binary matrix data in the main scanning direction in accordance with main-scanning direction pixel position information "Scanx" of the painting object under processing, which represents a first pixel position in the main scanning direction, the binary matrix data selection means 30q selects 32-bit binary matrix data SDs from the binary matrix data SDo and outputs the result, while successively shifting 180-bit binary matrix data SDo retained in the binary matrix data fetch register 22 bits at the steps of 32 bits till the halftone data generation process of a scan line under processing is completed.

How to selectively output the binary matrix data is shown in Fig. 41. Fig. 41 illustrates a case where a starting point (every 32 bits) of a pixel stream under processing of the painting

object, the data is read out of the output buffer memory 50q by the binary data write control circuit 40q; the readout data is bit inverted; the readout data and the inverted mask data are ANDed; and the result of the ANDing operation and the resulting of ANDing the binary matrix data SDs and the mask data "Mask" are stored into the output buffer memory 50q.

The halftone data stored into the output buffer memory 50q is transferred to the image recorder 200q where it is visualized as a halftone picture.

The output buffer memory 50q is a page memory in the embodiment, but it may be a band buffer memory. Where the band buffer memory is used for the output buffer memory, painting object data to be input to the halftone generation system 100q is divided into data blocks each of a predetermined band size. The data is processed every data block. At least two band buffer memories are provided. Those two band buffer memories are alternately subjected to the writing and reading of halftone data thereto and therefrom.

<Effects of the Ninth embodiment>

As described above, the binary matrix data which is as the result of binarizing using the threshold tone data and to be halftone data is directly read out of the output buffer memory 50q; the data read out of the output buffer memory is not the threshold tone data.

Therefore, the number of read data lines derived from the

222q. In operation, in response to the select signal RSEL the data selector 220q delivers the binary matrix data Binary matrix data SDo, which was read out, by 32bits, from the binary matrix data storage memory 10q, as binary matrix data SDo1 and SDo2 to the registers 221q and 222q..

The registers 221q and 222q are each formed with 32 number of D-flip-flop circuits. Fetch timing signals DFT1 and DFT2 are applied as clock signals to those flip-flop circuits of the registers 221q and 222q. In response to those fetch timing signals, the registers 221q and 222q hold the binary matrix data pieces SDo1 and SDo2 therein, and binary matrix data SDa of 64 bits as the combination of those data pieces SDo1 and SDo2 is input to a barrel shifter 32q to be described later.

<Selecting and Outputting of Binary Matrix Data>

The binary matrix data selection means 30q (Fig. 38) includes a binary-matrix-data select control circuit 31q, the barrel shifter 32q and a binary matrix data register 33q. To correct a shift of a pixel position of the painting object in the main scanning direction relative to a pixel position of the binary matrix data in the main scanning direction in accordance with main-scanning direction pixel position information "Scanx" of the painting object under processing, the binary matrix data selection means 30q selects 32-bit binary matrix data SDs from the binary matrix data SDa and outputs the result, while successively shifting 64-bit binary matrix data SDa retained in